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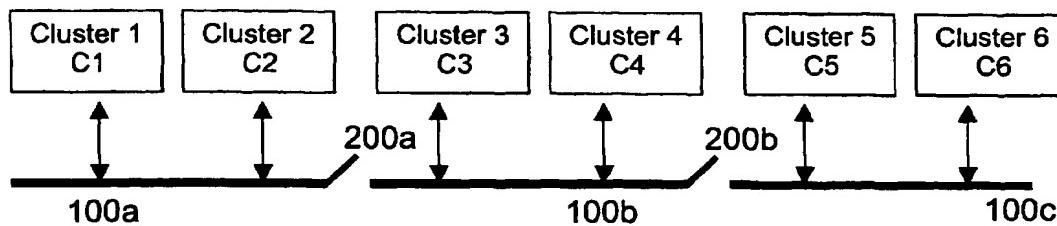
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(54) Title: CLUSTERED INSTRUCTION LEVEL PARALLELISM PROCESSOR



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(57) Abstract: The basic idea of the invention is to provide a clustered ILP processor based on a fully-connected inter-cluster network with a non-uniform latency. A clustered Instruction Level Parallelism processor is provided. Said processor comprises a plurality of clusters (C1 - C6) each comprising at least one register file (RF) and at least one functional unit (FU), wherein said clusters (C1 - C6) are fully-connected to each other; and wherein the latency of the connections between said clusters (C1 - C6) depends on the distance between said clusters (C1 - C6).



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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages   | Relevant to claim No. |
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| X          | US 5 475 857 A (DALLY WILLIAM J)<br>12 December 1995 (1995-12-12)<br>column 3, line 56 – column 4, line 22<br>column 5, line 30 – column 6, line 4<br>column 10, line 6 – line 50; figure 6<br>----- | 1-5                   |
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### **Information on patent family members**

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